

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
18 August 2005 (18.08.2005)

PCT

(10) International Publication Number
WO 2005/076681 A1

(51) International Patent Classification⁷: **H05K 3/46**,
3/18, 3/10

(21) International Application Number:
PCT/EP2005/000698

(22) International Filing Date: 20 January 2005 (20.01.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10 2004 005 300.6 29 January 2004 (29.01.2004) DE

(71) Applicant (for all designated States except US):
ATOTECH DEUTSCHLAND GMBH [DE/DE];
Erasmusstrasse 20, 10553 Berlin (DE).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **HOFMANN, Hannes**,
P. [DE/DE]; Mauchstrasse 8, 73525 Schwäbisch Gmünd
(DE).

(74) Agent: **EFFERT, BRESSEL UND KOLLEGEN**;
Radickestrasse 48, 12489 Berlin (DE).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,
MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,
PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM,
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,
ZW.

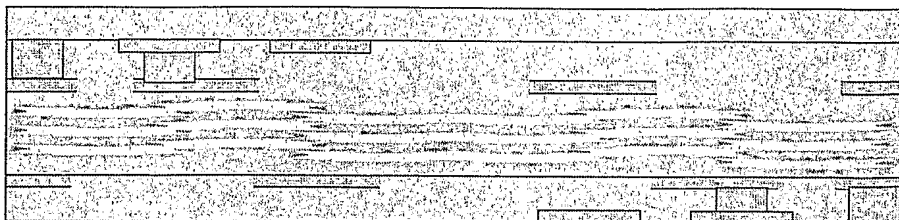
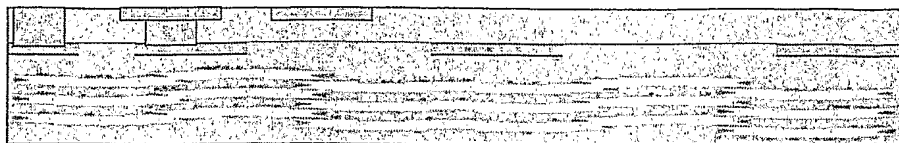
(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO,
SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MANUFACTURING A CIRCUIT CARRIER AND THE USE OF THE METHOD



(57) Abstract: A method of manufacturing a circuit carrier and the use of said method are proposed, said method comprising, after providing a printed circuit board (a), coating the circuit board on at least one side thereof with a dielectric (b), structuring the dielectric for producing trenches and vias therein using laser ablation (c) are performed. Next, a primer layer is deposited onto the dielectric, either onto the entire surface thereof or into the produced trenches and vias only (d). A metal layer is deposited onto the primer layer, with the trenches and vias being completely filled with metal for forming conductor structures therein (e). Finally, the excess metal and the primer layer are removed until the dielectric is exposed if the primer layer was deposited onto the entire surface thereof, with the conductor structures remaining intact (f).

WO 2005/076681 A1